# NI Multisim andExperimental Validation Implitation of Ratioed Logic Gates Using Memristor

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## ABSTRACT

Memristor is a two terminal fundamental passive element and hasbeen at the focus of several leading research groups, across the globe, in past few years.This paper demonstrates the design of logic gates using memristor. It will map to digital logic operation and how this can be used with Boolean logic.The logical operation of basic logic gates can be implemented practically using memristor and CMOS. The Simulations performed demonstrate the truth table for all logic gates and same have been verified experimentally on breadboard as well.

Keywords:Memristor,Mem-AND(Memristor AND),Mem-LOG gates (Logic gates),Mem-OR (Memristor OR) and Ni-Multisim.

## INTRODUCTION

There are two general types of components used in electronic i.e., passive (e.g. resistor,capacitor and inductor) and active (e.g.transistors and integrated circuits). Memristor are a new addition to this family which come under the category of passive elements.Memristor, a non linear (device) element, is an actively researched device now-a-days which was theoretically proposed by Leon Chua (1)in 1971 as the fourth circuit element besides the three well-known circuit elements; namely,resistor, capacitor and inductor.For a long time, it remained just as a theoretical element and rarely appeared in literature because of having no simple and practical realization and also because of its peculiar pinched hysteresis loop characteristics. In 2008, a group of researchers from HP laboratories(2)reportedfor the first time the fabrication feasibility of the device (having electrical characteristics similar to that of memristor) by growing $TiO_2$ thin film containing doped and un-doped regions between two metal contacts at nanometer scale. In past, several research groups have reported implementation of Digital Circuits based on Memristor through MATLAB Simulation(3-5) and SPICE modeling (6-7).

The MATLAB model(8-9) passes parameter for direct computation of various integral quantities such as voltage and current.

The theoretical proposed model of memristor given by HP labs has also been simulated using PSPICE (10).One of the major area of interest is the Ratioed logic gates by using Memristor.The basic Boolean logic operation AND, OR, NAND, NOT and XOR can be implemented with memristors. In the present work, the logic gates have been simulated using E.D.A. tool, NI Multisim (11) and experimentally verified on breadboard using discrete

components as given in (Table-I).AND and OR gates consist of two memristors connected in series, the only difference being that the two memristors are connected in a manner such that they have opposite polarity w.r.t where the inputs are applied.

Table-I components used with their respective values to implement the logic gates.

| Components | Values | Quantity(respective) |
|---|---|---|
| Resistor | 22kΩ,220Ω,3kΩ, 2kΩ | 2,2,1,1 |
| Op-amp | LMC6482AIN | 2 |
| J-K Flip-Flop | 7476 | 2 |

METHODOLOGY

The use of memristors to perform logical operations has been proposed in several different ways. In (12), memristors are used as a reconfigurable switch. Kvatinsky *et al*(13) presented a hybrid memristor-CMOS logic family: memristor ratioed logic (MRL) and recently reported Memristor-Based Material Implication (IMPLY) Logic (14). In the present work, a simplified approach has been used to implement Logic gates using memristors.Since memristor is not commercially available as a physical device, several emulator circuits have been proposed(15)(16) which generate the same characteristics of the device proposed by Leon Chua. We have used the two op-amp approach(15) to emulate memristor characteristics both in simulation as well as hardware implementation.
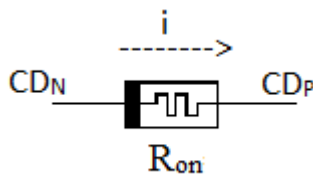
*Operation of Memristor*



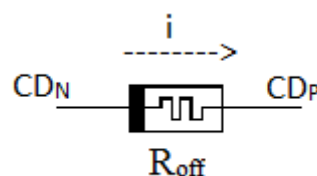Figure I Basic Chua's diode memristor symbol (direction of current from $CD_N$ to $CD_P$)

Figure II Basic Chua's diode memristor symbol (direction of current from $CD_N$ to $CD_P$)

Figure Iand IIshow the relationship of memristance with the direction of current or in other words the applied voltage. The memristance of a memristor is correspondingly set to the most($R_{on}$) or the least conductive state ($R_{off}$) depending on the direction of the current flow through it(17). When current flows from $CD_N$ to $CD_P$ (Figure I), the memristance is set to $R_{on}$, and when current flows from terminal $CD_P$ to $CD_N$ (Figure II) the memristance is set to $R_{OFF.}$ The off resistance is much greater than the on resistance i.e. , $R_{on} << R_{off.}$

*Mem-LOG Gates*
The Boolean logics can be designed using three methodologies i.e. Material Implication(IMPLY) based logic(14)(18),Memristor Ratioedlogic(19) and Memristor/CMOS Threshold logic(20).The CMOS Threshold logic is faster as compared with Ratioed logic but the ratioed logic is simpler.

*Mem-AND Gate*

The schematic diagram of two input AND gate(17)isas shown in (Figure III)where MR represents Memristor. MR0 and MR1 are two memristors connected in series. Inputs are applied to $CD_P$ terminals of individual memristors. Output is taken from $CD_N$ terminals connected together.
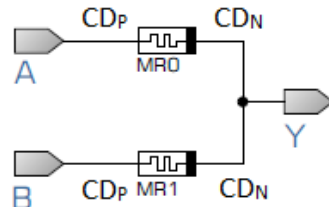


Figure III A logical AND operation using memristor as voltage divider.

*Working of Mem-AND*

The working of two input logic AND is explained below and is shown in (Figure IV)
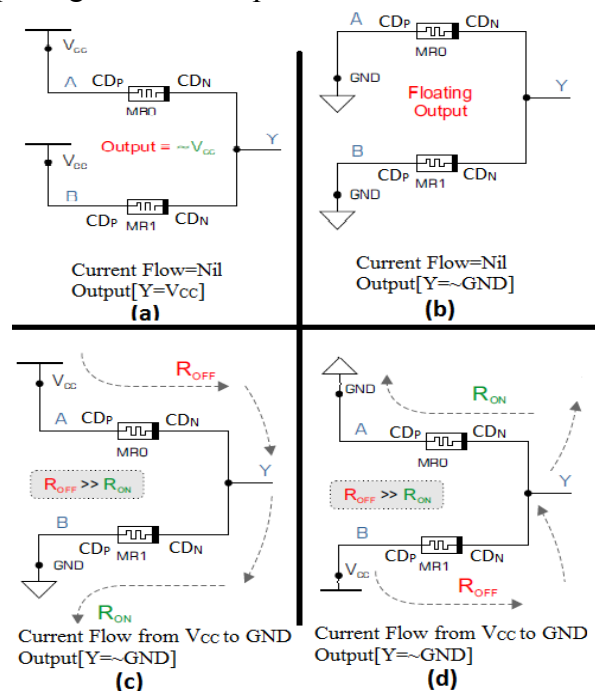


Figure IV Logic computation of AND gate using Memristors.

Case 1:Figure IV (a)

When input A=1($V_{CC}$) and input B=1($V_{CC}$) i.e., both the inputs are connected to 5V, both the memristors are at same potential. Both the memristors (MR0 &MR1) in the voltage divider circuit being at equipotential no current flows through them and thus the output will be high i.e.,Y= $V_{CC}$ or logic 1.

Case 2:Figure IV (b)

When input A=0 and input B=0,still no current flows through MR0and MR1 there is no potential difference across the voltage divider circuit and thereforeoutput Y= GND or logic 0.

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Case 3:Figure IV (c)

When input A=1 and input B=0 because of potential difference the current flows from $V_{cc}$ to GND in a direction such that the resistance of MR0 increases to a level $R_{off}$while the resistance of MR1 is decreased to a level say $R_{on}$. Output Y will be the voltage drop across MR1 memristor.From voltage divider rule,

$$Y = \frac{V_{CC} \times R_{on}}{R_{on} + R_{off}}$$

Since, $R_{on} \ll R_{off}$therefore $R_{off}+R_{on} \approx R_{off}$and hence $Y < Vcc \approx 0$.

Case 4: Figure IV (d)

When A=0 and B=1,currentwill still flow from $V_{cc}$ to GND, because of potential differencebut now the resistance of MR1 increases to a level $R_{off}$while the resistance of MR0 is decreased to a level $R_{on}$The output will now be the voltage drop across memristor MR0.From voltage divider rule,

$$Y = \frac{V_{CC} \times R_{on}}{R_{on} + R_{off}}$$

Since, $R_{on} \ll R_{off}$therefore $R_{off}+R_{on} \approx R_{off}$and hence $Y < Vcc \approx 0$.

(Figure V) shows the NI-Multisim implementation of logic AND using two memristors MR0 and MR1 where each memristor is implemented by the two op-amp emulator circuit. The 2-bit counter is used to generate all four possible input combinations(00,01,10,11) asinputs to the AND  gate.
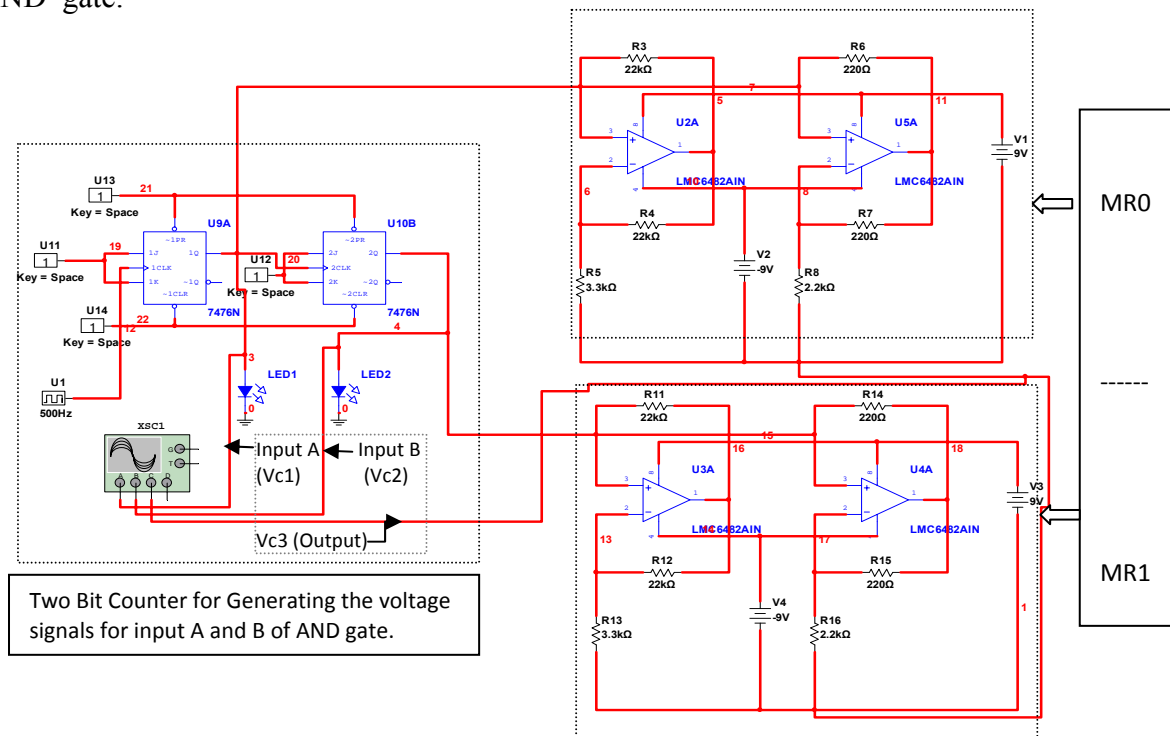


Figure V Implementation of AND gate through Memristor through Multisim.

(Figure VI) shows simulated output waveform of logic AND gate verifying the truth table for logic AND operation where,
Vc1 - Voltage signal to the input A of the gate.
Vc2 – Voltage signal to the input B of the gate.
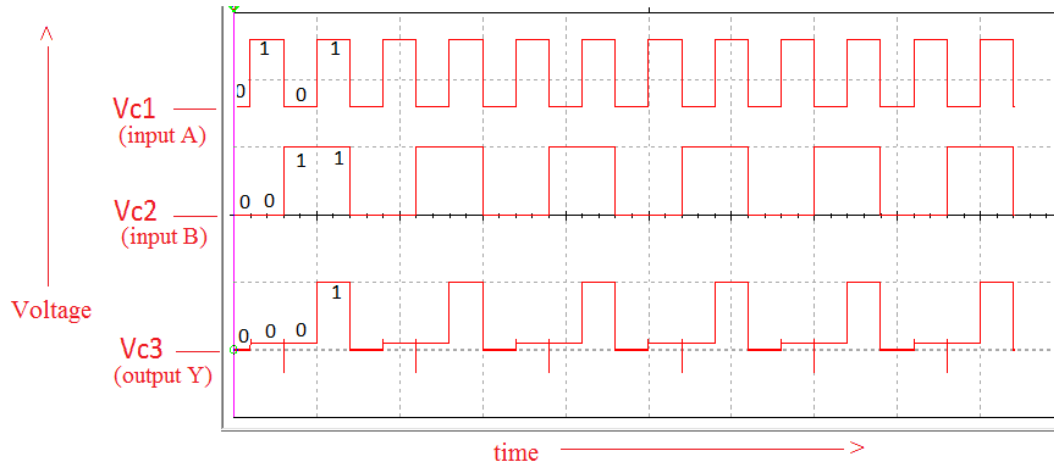Vc3 – Voltage signal at the output of logic AND gate.



Figure VI Timing waveform (Simulated) of AND gate where Vc1 and Vc2 are the voltage signals of input A and input B for two input Mem-AND, Vc3 represents the output of AND gate.

(Table-II) shows theVoltage Levels at the Output of Different Op-Amps in (Figure V) where in the two op-amp emulator circuit of Chua's Diode (Memristor)U2A is theFirst op-amp of MR0 &U5A is the Second op-amp of MR0.Similarly, U3A isthe First op-amp of MR1 &U4A isthe Second op-amp of MR1.

Table II Representing the Voltage Level at the Outputs of Logic AND and Different Op-Amps of (Figure V).

| A | B | AND Gate(Output) | | U2A | | U5A | | U3A | |
|---|---|---|---|---|---|---|---|---|---|
| | | Sim. | Exp. | Sim. | Exp. | Sim. | Exp. | Sim. | Exp. |
| 0 | 0 | 1.03mV | 1.16mV | 2.70mV | - 7.05mV | 1.04mV | -27.8mV | 2.71mV | -7.06mV |
| 0 | 1 | 2.30V | 3.20V | -8.11V | -7.10V | -230mV | -320mV | 8.11V | 8.21V |
| 1 | 0 | 2.30V | 4.2V | 8.11V | 8.2V | 5.27V | 5.20V | -8.11V | -7.00V |
| 1 | 1 | 5.00V | 5.88V | 5.00V | 5.86V | 5.00V | 5.09V | 5.00V | 6.20V |

Close proximity of simulated results with experimental results validates the implementation topology of AND gate using memristors.

Experimental Set-Up for Mem-OR realization

*Operation of Mem-OR Gate*
(Figure VII) shows the experimental set-up.The schematic diagram of two inputs OR gate (17) is as shown in (Figure VIII) where MR represents Memristor. MR0 and MR1 are two memristors connected in series. Inputs are applied to $CD_N$ terminals of individual memristor. Output is taken from $CD_P$ terminals connected together.
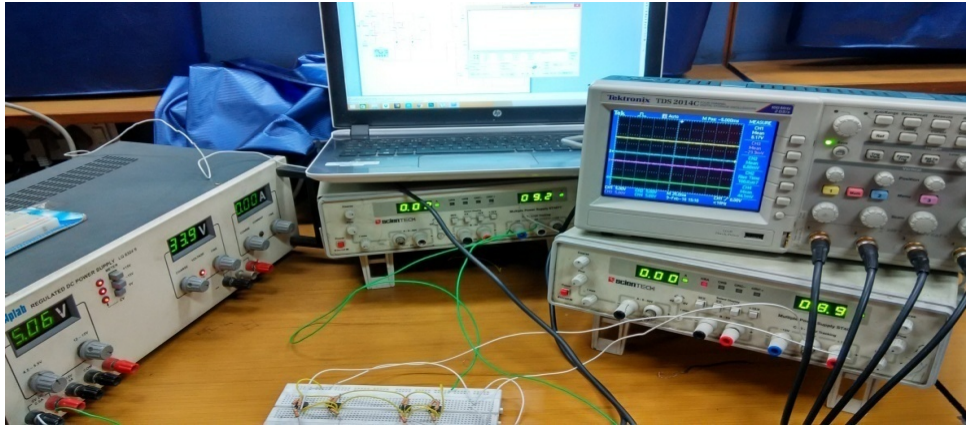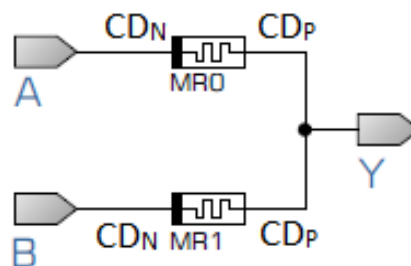
Figure VII Experimental Set Up



Figure VIII A logical OR operation using memristors.

The working of logic for four input combinations is explained below and is graphically represented in (Figure IX).

Case 1: Figure IX (a)

When input A=1($V_{CC}$) and input B=1($V_{CC}$) i.e.,both the input are connected to 5V, thus both the memristor are at same potential and hence no current flows through the memristors and output will be connected to high i.e., Y= $V_{CC}$ or logic 1.

Case 2: Figure IX (b)

When input A=0 and input B=0,being at equipotential no current flows through the circuit and therefore output Y= GND or logic 0.

Case 3: Figure IX (c)

When input A=1 and input B=0,the current flows from $V_{cc}$ to GND in a direction such that the resistance of MR0 decreases to a level $R_{on}$ while the resistance of MR1 is increased to a level say$R_{off}$The output will now be the voltage drop across memristor MR1. From voltage divider rule,

$$Y = \frac{V_{CC} \times R_{on}}{R_{on} + R_{off}}$$

Since, $R_{on}$<< $R_{off}$therefore$R_{off}$+$R_{on}$≈$R_{off}$and hence Y =Vcc .

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Case 4: Figure IX (d)

When input A=0 and input B=1, current still flows from $V_{cc}$ to GND, but the resistance of MR1 decreases to a level $R_{on}$ while the resistance of MR0 is increased to a level $R_{off}$ output will now be given by the voltage drop across MR0. From voltage divider rule,

$$Y = \frac{V_{CC} \times R_{on}}{R_{on} + R_{off}}$$

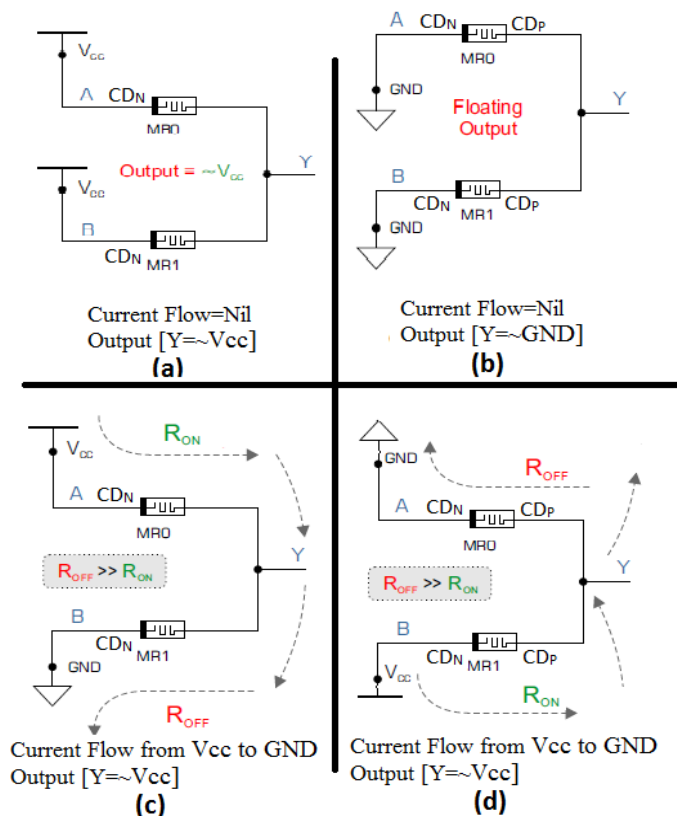Since, $R_{on} << R_{off}$ therefore $R_{off} + R_{on} \approx R_{off}$ and hence Y = Vcc .



Figure IX Logic computation of OR gate using Memristors.

(Table-III) shows theVoltage Level at the Output of Different Op-Amps of (Figure X). Close proximity of simulated results with experimental results validates the implementation topology of OR gate using memristors.

Table-III Representing the Voltage Level at the Outputs of Logic OR and Different Op-Amps as shown in (Figure X).

| A | B | OR Gate(Output) | | U2A | | U5A | | U3A | |
|---|---|---|---|---|---|---|---|---|---|
| | | Sim. | Exp. | Sim. | Exp. | Sim. | Exp. | Sim. | Exp. |
| 0 | 0 | -8.13V | -8.11V | -8.17V | -8.13V | -8.11V | -8.16V | -8.11V | -8.15V |
| 0 | 1 | 8.19V | 8.20V | 8.12V | 8.06V | 8.11V | 8.33V | 8.11V | 8.21V |
| 1 | 0 | 8.11V | 8.19V | 8.12V | 8.18V | 8.11V | 8.38V | 8.11V | 8.22V |
| 1 | 1 | 8.11V | 8.20V | 8.11V | 8.38V | 8.12V | 8.11V | 8.11V | 8.20V |

(Figure X) shows NI-Multisim implementation of logic OR using two memristors MR0 and MR1. The 2-bit counter is used to generate all four possible input combinations(00,01,10,11) for OR gate, whereas (Figure XI) shows simulated output waveform of logic AND gate verifying the truth table for logic AND operation., where,

    Vc1 - Voltage signal to  input A of the gate.
    Vc2 – Voltage signal to input B of the gate.
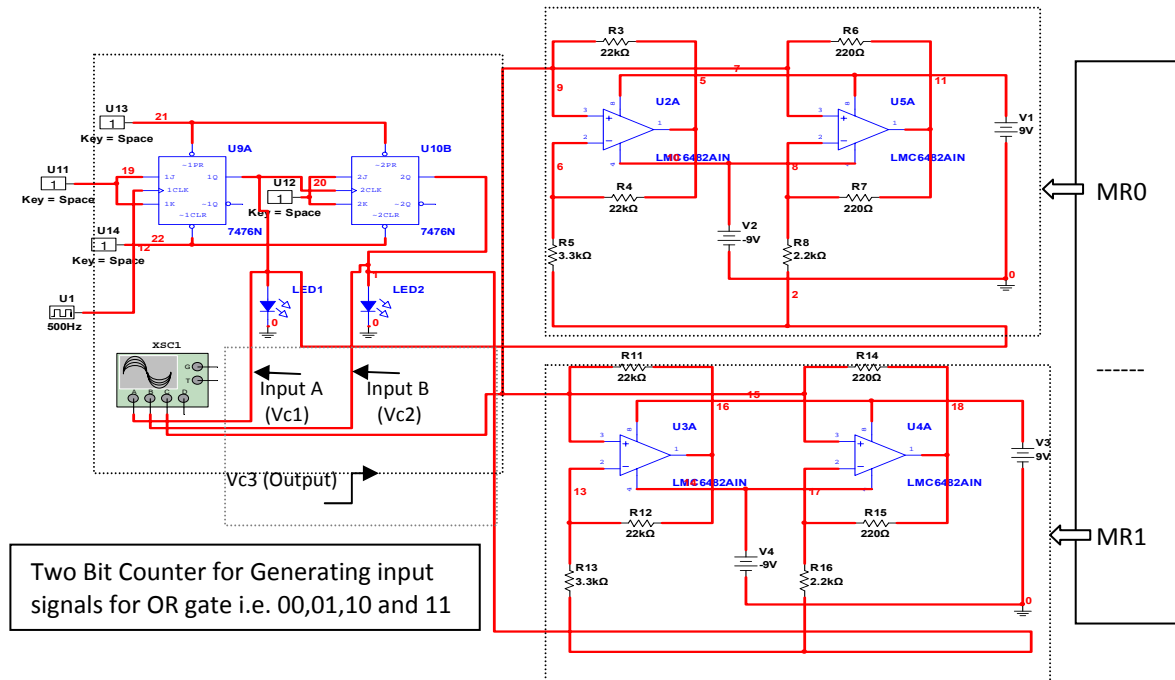    Vc3 – Voltage signal at output of logic AND



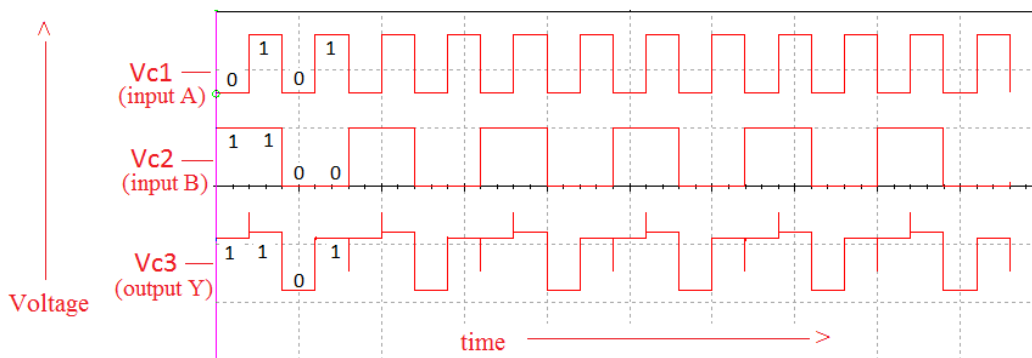Figure X Simulation circuit diagram of OR gate using memristor.



Figure XI Timing waveform (Simulated) of OR gate where Vc1 and Vc2 are the voltage signals of input A and input B for two input Mem-AND, Vc3 represents the output of OR gate.

## Logical Implementation of Mem-NAND and Mem-NOR

(Figure XII and XIII) represents logical NAND and NOR gate implementation using memristors and CMOS inverter. For the case of NAND gate when A=1 and B=1,no current flows through circuit. The output of AND gate is logic 1 which is inverted by CMOS inverter and hence produces the output Y=GND. For the case when A=0 and B=0, the output before

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CMOS inverter is 0 and the final output is Y=Vcc or logic 1. For the case when either of the input is connected to Vcc while the other input is grounded, the logic 1 is obtained as output and hence verifies its truth table.
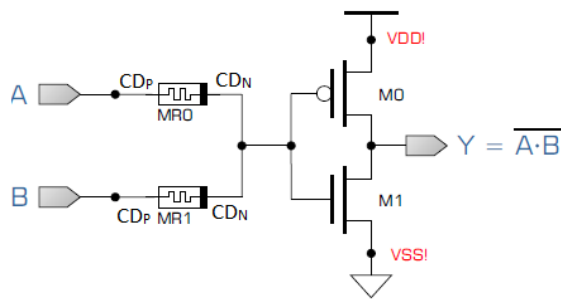


Figure XII A logical NAND gate using memristorsand CMOS inverter
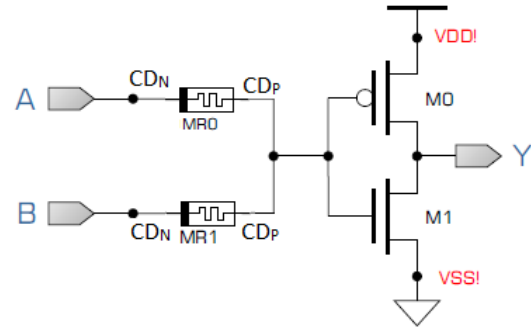
Figure XIII A logical NOR gate using memristors and CMOS inverter

(Table-IV) shows the simulated results of the NAND and NOR gate and the output voltage levels shows that the simulated results are in consonance with the ideal truth table of the logic gates.

Table-IV represents the simulated results of NAND and NOR gate using NI Multisim.

| A | B | NAND | | NOR | |
|---|---|---|---|---|---|
| 0 | 0 | LOGIC 1 | 5.00V | LOGIC 1 | 5.00V |
| 0 | 1 | LOGIC 1 | 3.71V | LOGIC 0 | 1.13V |
| 1 | 0 | LOGIC 1 | 3.71V | LOGIC 0 | 1.13V |
| 1 | 1 | LOGIC 0 | 50nV | LOGIC 0 | 5.30uV |

## RESULTS

In this paper, implementation of memristor based AND and OR gate have been demonstrated through NI Multisim and results so obtained are in consonance with the experimental results.

## DISCUSSION

The fourth basic circuit element was proposed in 1971 by Leon Chua and was first manufactured in 2008 by HP labs. Memristor which is a two terminal now fundamental electronic device is passive in nature and exhibits non-linear dynamics. Memristor which does have a potential in the analog domain but here it is used as a two state switch for binary digital application depending upon the another state $R_{on}$ /$R_{off}$ polarity of the applied voltage and the direction of current through it its potential to shift its memresistance value from one state $R_{off}$ / $R_{on}$ to another state $R_{on}$ /$R_{off}$ makes it a simple device to implement binary logic. Though compliment is not possible with memristor, but because of its compatibility with CMOS integration, the complete set of Boolean logic can be implemented using memristors.
In the work presented our focus has been on implementation, realization, functioning and analysis of memristor and memristive circuits in the binary domain with discrete components and actual circuits rather than focusing only on the computational methods of analysis. In the

present work op-amps have been used to emulate memristors which are then further used to implement various logic gates and the truth tables have been verified experimentally as well. The spikes observed in the simulation are due to parasitic capacitances.

CONCLUSIONS

In the present work, implementation of logic gates using Memristors has been presented. The close agreement of the simulated results of the AND and OR gate with the experimental results validates the approach and the approach can be extended to make combinational and sequential circuits.

ACKNOWLEDGMENTS

REFERENCES

1. Chua L. O. (1971), Memristor - the missing circuit element,*IEEE Trans. on Circuit Theory*, Vol: 18(5), pp. (507–519).
2. Strukov Dmitri B., Snider Gregory S., Stewart Duncan R. and Stanley R. Williams (2008), The missing memristor found, *Nature* 453, (80– 83)
3. Shultz Kenneth M., Memristors (2009) (https://kennethmichael.files.wordpress.com/2010/08/memory-resistors-2009.pdf )
4. Gale Ella, Ben de Lacy Costello., Adamatzky Andrew, Boolean Logic Gates From A Single Memristor Via Low-Level Sequential Logic (February 18, 2014) (http://arxiv.org/pdf/1402.4046.pdf )
5. Rajbala, Saini Sanju (2014), MATLAB implementation of memristor based chua's circuit and its chaos control, *Int. J. of Recent Trends in Engineering & Technology*, Vol. 11, pp.(484-492).
6. Biolek Zdeněk, Biolek Dalibor, Biokova Viera(2009), SPICE Model of Memristor with Nonlinear Dopant Drift, *Radioengineering*, Vol: 18, No. 2, pp. (210-214) (http://www.radioeng.cz/fulltexts/2009/09_02_210_214.pdf)
7. Mladenov Valeri M. and Kirilov Stoyan M., Memristor (2015), Modeling In MATLAB & PSPICE, *29th European Conference on Modelling and Simulation, ECMS 2015, Albena (Varna), Bulgaria, May 26-29, 2015. Proceedings. European Council for Modeling and Simulation*, pp.(432-437) (http://www.scs-europe.net/dlib/2015/ecms2015acceptedpapers/0432-simo_ECMS2015_0032.pdf )
8. Singh Jeetendra lekhraj and Kakde Manoj S. (2014), Memristor matlab modeling, *International Journal of Engineering Research & Technology (IJERT)*, Vol: 3 (7), pp. (191-194).
9. Zaplatilek Karel (2011), Memristor modeling in MATLAB & Simulink, *ECC'11 Proceedings of the 5th European conference on European computing conference*, pp. (62-67). (http://www.wseas.us/e-library/conferences/2011/Paris/ECC/ECC-08.pdf )
10. Bhave Ketaki and Sarwade Nisha (2014), Memristor Modeling Using PSPICE. *Int. Journal of Engineering Research and Applications*, Vol: 4, Issue 7, pp.(139-143). (http://www.ijera.com/papers/Vol4_issue7/Version%203/X04703139143.pdf )
11. NI Multisim Education Edition Version 13.0, Lic. Serial No.: M79X04290

12. Strukov D. B. and. Likharev K. K (2005), CMOS FPGA: A reconfigurable architecture for hybrid digital circuits with two-terminal nanodevices, *Nanotechnology*, Vol: 16, no. 6, pp. (888–900)
13. Kvatinsky S., Wald N., Satat G., Friedman E. G., Kolodny A. and Weiser U. C., (2012) MRL – Memristor Ratioed Logic (http://webee.technion.ac.il/people/skva/MRL_for_pdf.pdf)
14. Kvatinsky Shahar, Satat Guy, Wald Nimrod,. Friedman Eby G, Kolodny Avinoam and Weiser Uri C. (2014), Memristor-Based Material Implication (IMPLY) Logic: Design Principles and Methodologies, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 22, No. 10. pp. (2054 - 2066).
15. http://nonlinear.eecs.berkeley.edu/chaos/chaos.html,2009.

16. Chen Mo, Yu Jingjing, Yu Qing, Li Changdi and Bao Bocheng (2014),A Memristive Diode Bridge-Based Canonical Chua's Circuit, *Entropy*, Vol: 16, pp. (6464-6476); doi:10.3390/e16126464

17. Vourkas Ioannis and Sirakoulis Georgios Ch. (2016), Memristor-Based Nanoelectronic Computing Circuits And Architectures, *Springer International Publishing Switzerland*, Hardcover ISBN 978-3-319-22646-0

18. Raghuvanshi Anika and Perkowski Marek (2014), Logic synthesis and a generalized notation for memristor-realized material implication gates, *Proceeding ICCAD '14 Proceedings of the 2014 IEEE/ACM International Conference on Computer-Aided Design,* pp. (470-477)

19. Kvatinsky S., Wald N., Satat G., Kolodny A., Weiser U. C., Friedman E. G., MRL — Memristor Ratioed Logic, *13th International Workshop on Cellular Nanoscale Networks and Their Applications (CNNA),*Turin, 2012, pp. 1-6. doi: 10.1109/CNNA.2012.6331426

20. Ligang Gao, Alibart F., Strukov D. B.(2013), Programmable CMOS/Memristor Threshold Logic, *IEEE Transactions on Nanotechnology*, Vol: 12, no.2, pp.(115-119). doi: 10.1109/TNANO.2013.2241075